CLAIMS

What is claimed is:

1. A method for fabricating a flash memory device comprising:

fabricating a gate structure comprising a tunnel oxide layer, a floating gate layer, an oxide layer, and a control gate layer on a semiconductor substrate; and

repairing said tunnel oxide layer using a rapid thermal oxidation (RTO) process.

2. The method as recited in Claim 1, further comprising:

creating a first impurity concentration in said semiconductor substrate prior to said repairing; and

creating a second impurity concentration in said semiconductor substrate prior to said repairing.

3. The method as recited in Claim 2, wherein said fabricating comprises fabricating a gate structure that is less than 0.21 microns (0.21μ) in length.

4. The method as recited in Claim 1, wherein said repairing comprises:

creating additional oxide material in a damaged region of said oxide layer.

5. The method as recited in Claim 1, wherein said rapid thermal oxidation process comprises exposing said semiconductor structure to a temperature of 1000° C for a period of time not longer than 20 seconds.

6. The method as recited in Claim 1, wherein said rapid thermal oxidation process comprises selecting a plurality of process parameters wherein a portion of said tunnel oxide layer retains a uniform profile after said rapid thermal process is performed.

7. A method for fabricating a memory device comprising:

fabricating a gate structure upon a semiconductor substrate;

depositing a dopant in a first region of said semiconductor substrate and in a second region of said semiconductor substrate; and

performing a rapid thermal oxidation (RTO) process upon said semiconductor substrate.

8. The method as recited in Claim 7, wherein said memory device comprises a flash memory device and comprising fabricating a floating gate memory structure upon said semiconductor substrate.

9. The method as recited in Claim 8, wherein said fabricating comprises fabricating a floating gate structure that is than 0.21 microns (0.21μ) in length.

10. The method as recited in Claim 7, wherein said performing a rapid thermal oxidation process comprises creating additional oxide material in a damaged region of an oxide layer of said floating gate structure.

11. The method as recited in Claim 11, wherein said rapid thermal oxidation process comprises selecting a plurality of process parameters wherein a portion of said tunnel oxide layer retains a uniform profile after said rapid thermal process is performed.

12. The method as recited in Claim 11, wherein said rapid thermal oxidation process comprises exposing said semiconductor structure to a temperature of 1000° C for a period of time not longer than 20 seconds.

13. A method for fabricating a memory device comprising:

depositing a plurality of layers upon a semiconductor substrate;

patterning said plurality of layers to create a stack gate; and

performing a rapid thermal oxidation (RTO) upon said stack gate.

14. The method as recited in Claim 13, further comprising:

creating a source region wherein a first impurity concentration is deposited in said semiconductor substrate; and

creating a drain region wherein a second impurity concentration is deposited said semiconductor substrate.

15. The method as recited in Claim 14, wherein said patterning comprises creating a stack gate upon said semiconductor substrate that is less than 0.21 microns (0.21μ) in length.

16. The method as recited in Claim 13, wherein said performing a rapid thermal oxidation comprises:

creating additional oxide material in a damaged region of an oxide layer of said stack gate.

17. The method as recited in Claim 16, wherein said rapid thermal oxidation process comprises selecting a plurality of process parameters wherein a portion of said tunnel oxide layer retains a uniform profile after said rapid thermal process is performed.

18. The method as recited in Claim 17, wherein said rapid thermal oxidation process comprises exposing said semiconductor structure to a temperature of 1000° C for a period of time not longer than 20 seconds.